REMARKS

Claims 1-4, as amended, remain herein.

Claims 1-4 have been amended to recite more clearly applicant's invention. See applicant's specification at page 12, lines 7-25.

This Amendment places all claims 1-4 in condition for allowance, and surely in better condition for any appeal. Thus, entry of this Amendment and allowance of all claims 1-4 are respectfully requested.

1. Claims 1-4 were rejected under 35 U.S.C. §103(a) over Endoh et al. U.S. Patent 5,485,094 and Ferguson et al. U.S. Patent 6,202,181.

The presently claimed inspection method comprises counting input logical values, such that one of the adjacent lines has a logical value "1", while the other has a logical value "0", simultaneously with detection of stuck-at failures, and selecting the input logical values of lines of the logical circuit other than the adjacent lines, such that an output logical value that is expected when the input logical values

setting a pair of the logical values "0" and "1" are input to the logical circuit, is changed by a short circuit of the adjacent lines. This method is nowhere disclosed or suggested in any of the cited references.

The Office Action cites Endoh '094 as allegedly disclosing a method for detecting short circuit failures between device lines, obtaining input logical values such that one of the adjacent lines has a logical value "1" while the other has a logical value "0", monitoring an output of a logical circuit that receives the input logical values, and comparing the monitored output with an output logical value that is expected when the input logical values are input to the logical circuit.

The Office Action cites Ferguson '181 as allegedly teaching extracting adjacent lines from the physical layout pattern and judging a short circuit failure.

In contrast, the presently claimed method comprises extracting not only adjacent lines and setting one of them to the logical value "0" while the other of them is set to the logical value "1", thereby detecting any short circuit failure, but also the steps of, as a procedure for setting the logical

values of "0" and "1", (1) noticing a pair of lines having a possibility that a short circuit failure may occur, (2) selecting the input logical values which the pair can detect, and (3) selecting the logical values of the other lines such that the output logical values that are expected from pairs of the input logical values are changed by the change of the input logical value.

These steps are described in the specification at page 12, lines 7-25, describing first selecting the combination of lines 251 and 254, and setting one of the logical values "0" and "1" for input terminal 201, and the other of the logical values to input terminal 204 (step S202). In such a case, input terminal 201 is connected to three-input AND gate 210 of Fig. 2. Since the output E of three-input AND gate 210 is affected also by inputs B and C to input terminals 202 and 203, respective inputs B and C to input terminals 202 and 203 are set to the logical values "1" such that output E of three-input AND gate 210 is changed by input A to input terminal 201 (step S203). When these values are set, the value of the output obtained when there is a short circuit failure between lines 251 and 254 is

different from the value in the case including no short circuit failure. Then, the correct output logical values that are expected from the set of input logical values are obtained (step S204). Figure 5(a) shows the truth table that is obtained in this way.

Endoh '094 does not disclose or suggest the above steps for inspecting a semiconductor and Ferguson '181 does not provide the deficiencies of Endoh '094 described herein.

For the foregoing reasons, neither Endoh '094 nor Ferguson '181 contains any teaching, suggestion, reason, motivation or incentive that would have led one of ordinary skill in the art to applicant's claimed invention. Nor is there any disclosure or teaching in either of these references that would have suggested the desirability of combining any portions thereof effectively to anticipate or suggest applicant's presently claimed invention. Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

All claims 1-4 are now proper in form and patentably distinguished over all grounds of rejection cited in the Office Action. Accordingly, allowance of all claims 1-4 is respectfully requested.

Should the Examiner deem that any further action by the applicant would be desirable to place this application in even better condition for issue, the Examiner is requested to telephone applicant's undersigned representatives.

Respectfully submitted,

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December 22, 2003
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